DESCRIPTOR WRITE BACK DELAY MECHANISM TO IMPROVE PERFORMANCE

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ABSTRACT OF THE DISCLOSURE

[0138] A multiprocessor switching device substantially implemented on a single CMOS integrated circuit is described in connection with a descriptor write back timer mechanism for use in efficiently writing descriptors back to memory after transmitting data under control of the descriptors to inform the processor(s) about system-related functions for a plurality of channels. A timing interval pulse is provided for prompting descriptor write back operations that are otherwise subject to a minimum descriptor count requirement.